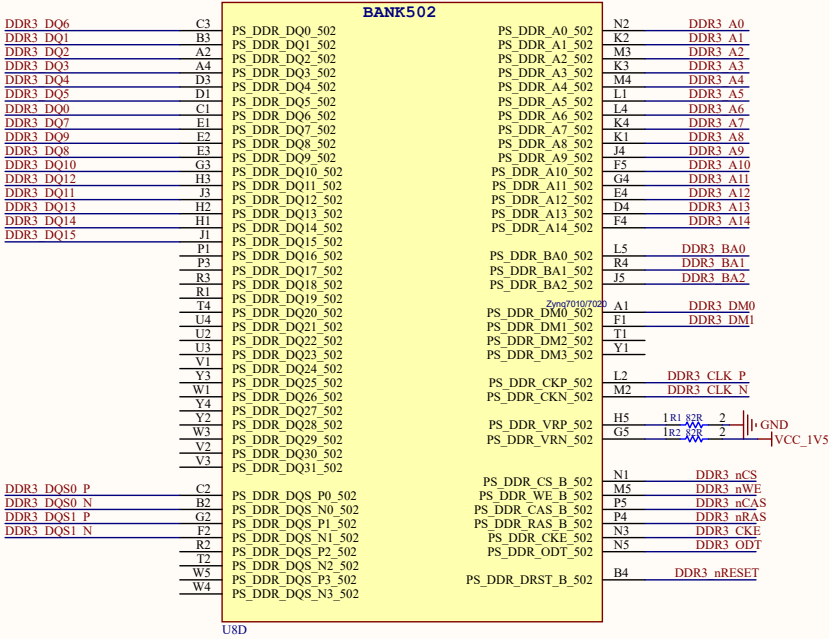
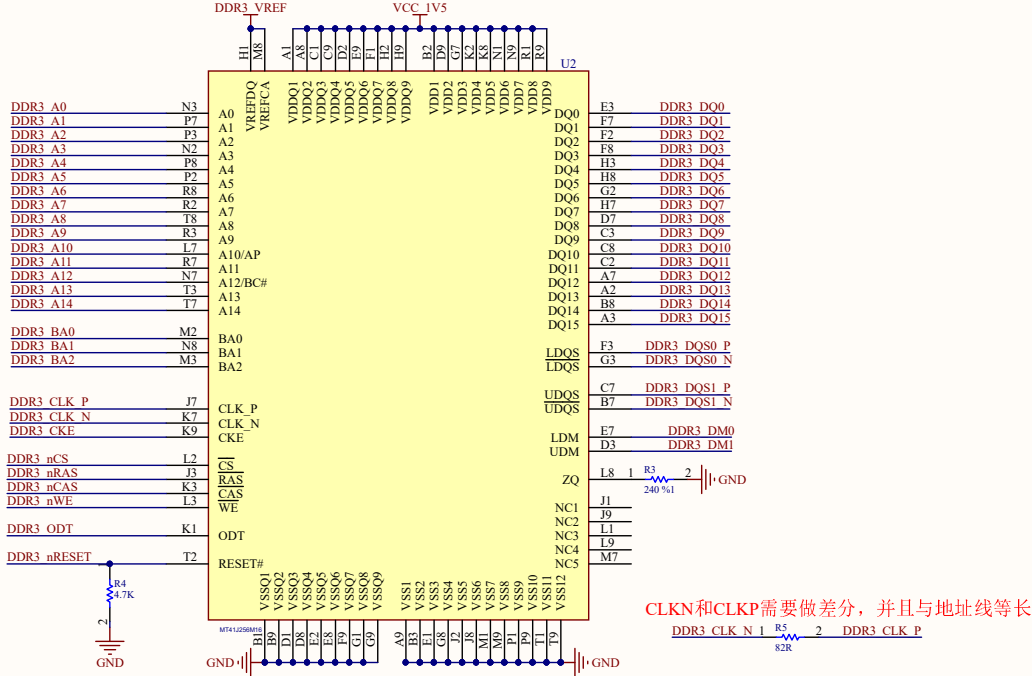
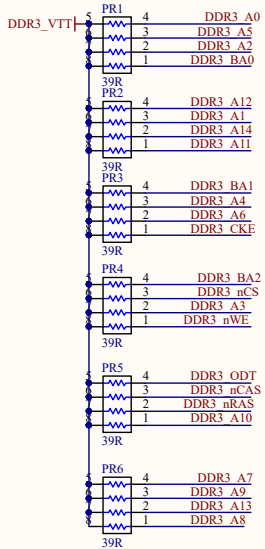


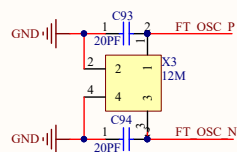
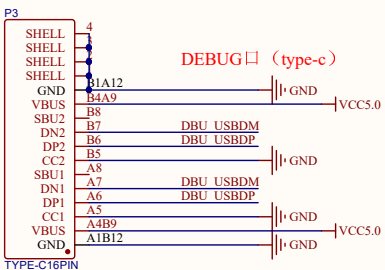
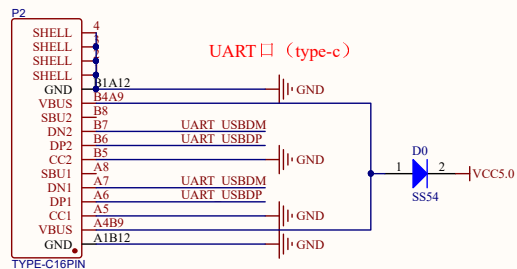
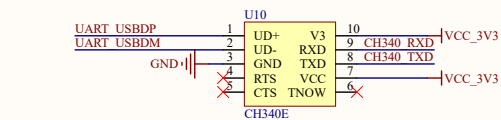
DDR3的DQ和DQS, DM等长, DQSP和DQSN还需要做差分



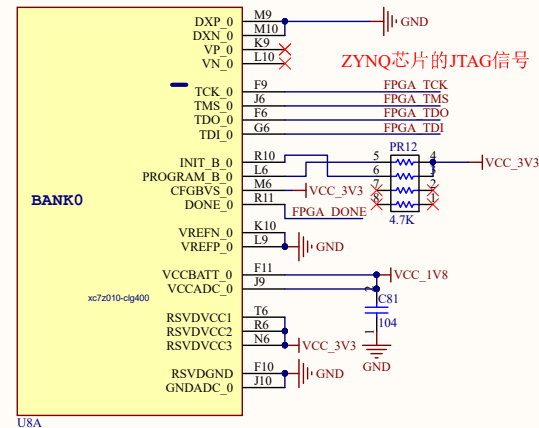
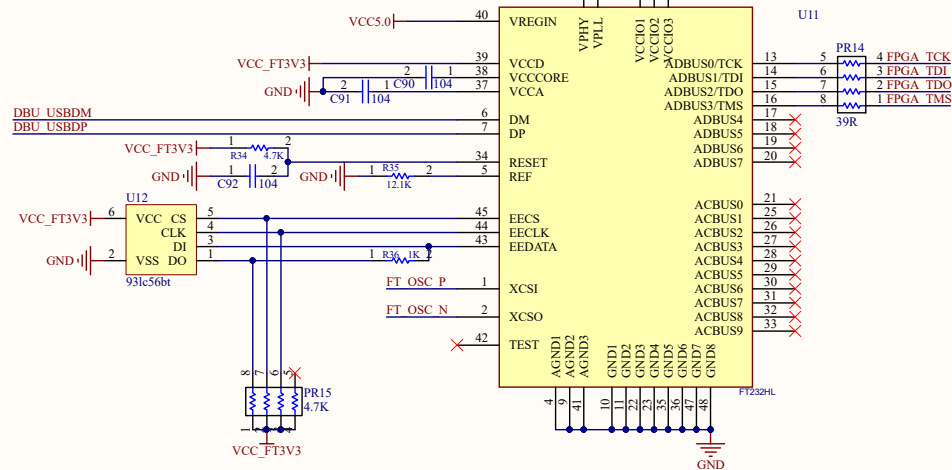
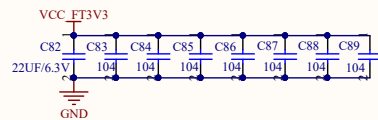
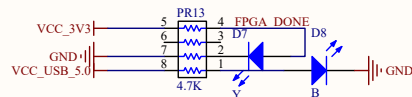
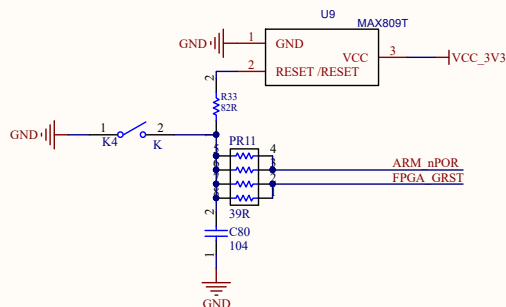
A0-A14以及其控制线需要做等长, 并且终端需要匹配39R电阻上拉到VTT



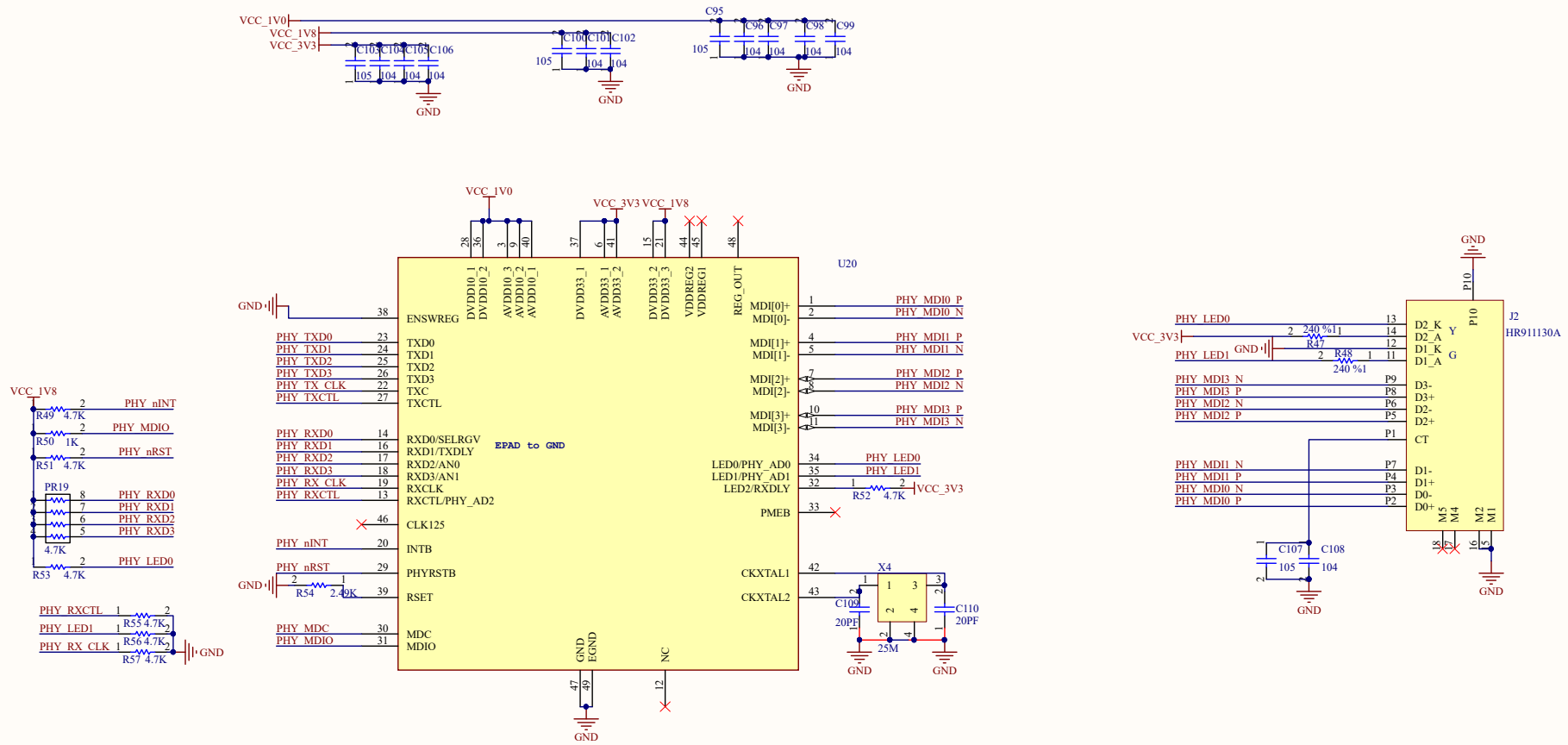
CLKN和CLKP需要做差分, 并且与地址线等长

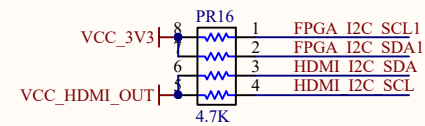
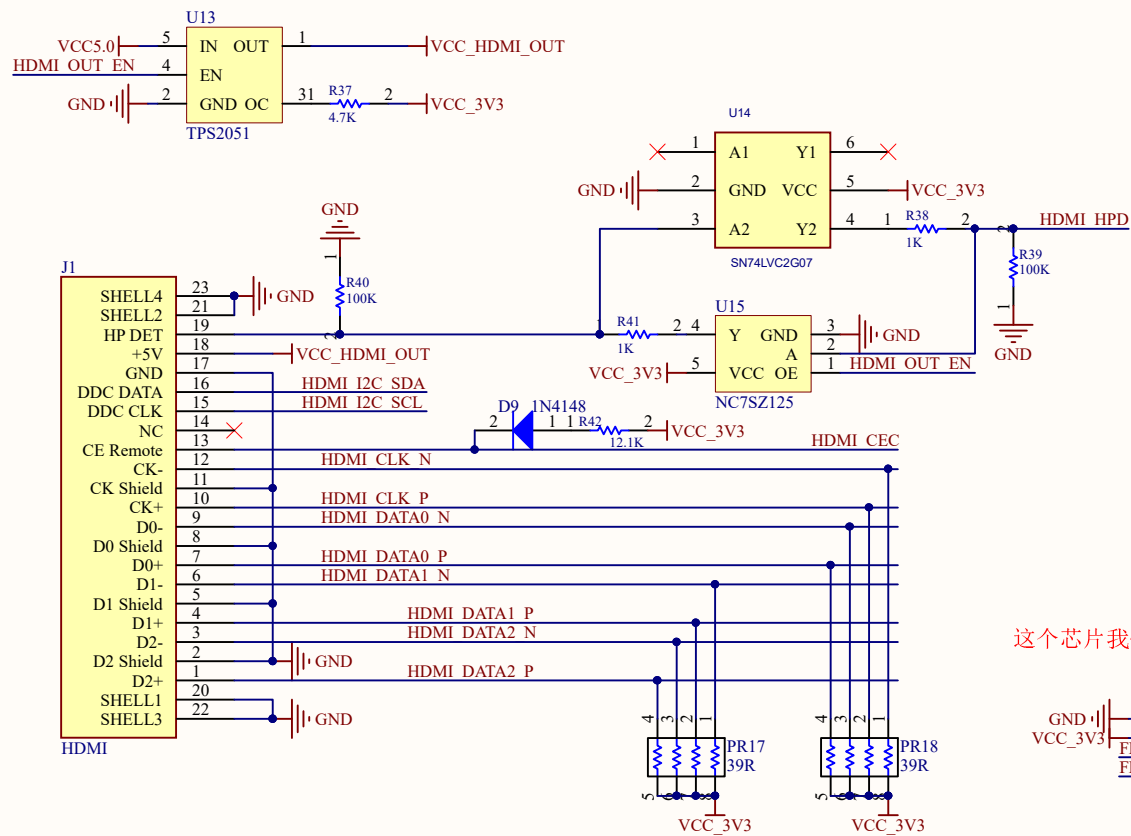


上电复位芯片，检测到3.3电源电压就绪产生一个拉低复位

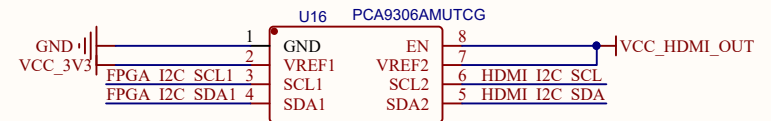


调试芯片的JTAG信号

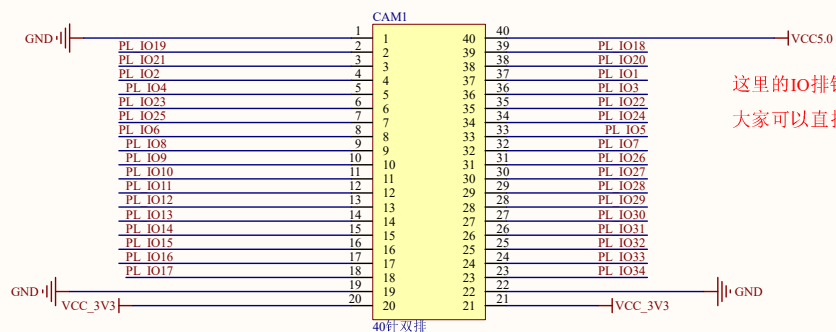




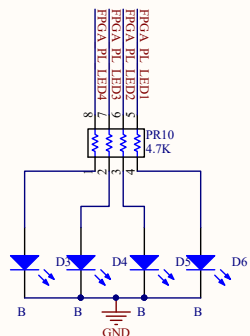
这个芯片我们用不到，实际没有焊接，我们HDMI主动输出显示信号，不需要IIC通信



IIC电平转换器

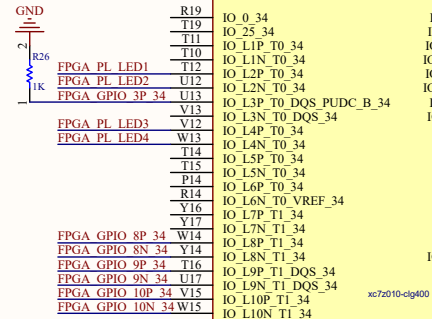
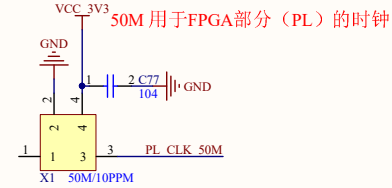


EXT IO	
V5.0	GND
P15	U15
V15	W15
V17	U17
Y18	V18
Y19	W18
W19	U19
N17	U14
W14	Y14
P16	V16
R16	U18
T16	T17
W16	R17
R18	W20
P19	V20
P18	U20
N18	T20
N20	P20
GND	GND
V3.3	V3.3

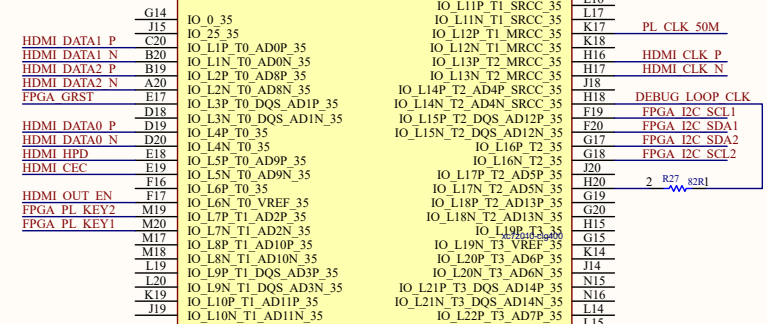


FPGA GPIO 21P 34	PL IO1
FPGA GPIO 9N 34	PL IO2
FPGA GPIO 17P 34	PL IO3
FPGA GPIO 21N 34	PL IO4
FPGA GPIO 23P 34	PL IO5
FPGA GPIO 11P 34	PL IO6
FPGA GPIO 8P 34	PL IO7
FPGA GPIO 8N 34	PL IO8
FPGA GPIO 18P 34	PL IO9
FPGA GPIO 12P 34	PL IO10
FPGA GPIO 20P 34	PL IO11
FPGA GPIO 19N 34	PL IO12
FPGA GPIO 16N 34	PL IO13
FPGA GPIO 16P 34	PL IO14
FPGA GPIO 15N 34	PL IO15
FPGA GPIO 15P 34	PL IO16
FPGA GPIO 14N 34	PL IO17

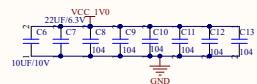
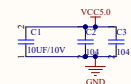
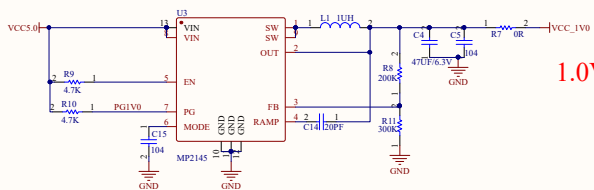
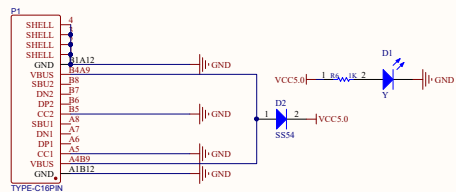
PL IO18	FPGA GPIO 24P 34
PL IO19	FPGA GPIO 11N 34
PL IO20	FPGA GPIO 10P 34
PL IO21	FPGA GPIO 10N 34
PL IO22	FPGA GPIO 17N 34
PL IO23	FPGA GPIO 22P 34
PL IO24	FPGA GPIO 22N 34
PL IO25	FPGA GPIO 12N 34
PL IO26	FPGA GPIO 24N 34
PL IO27	FPGA GPIO 19P 34
PL IO28	FPGA GPIO 9P 34
PL IO29	FPGA GPIO 18N 34
PL IO30	FPGA GPIO 20N 34
PL IO31	FPGA GPIO 13N 34
PL IO32	FPGA GPIO 23N 34
PL IO33	FPGA GPIO 13P 34
PL IO34	FPGA GPIO 14P 34



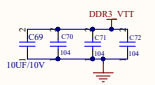
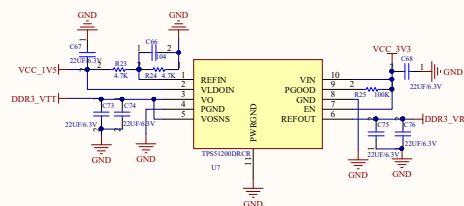
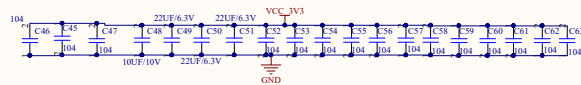
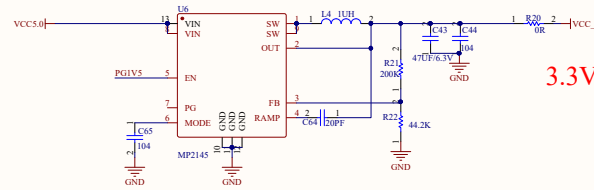
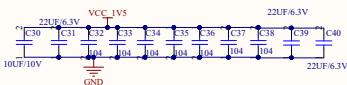
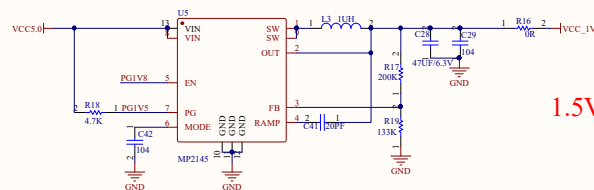
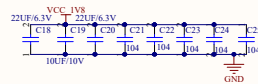
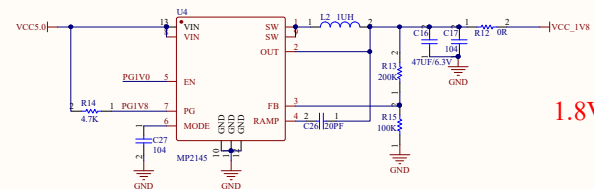
U8F

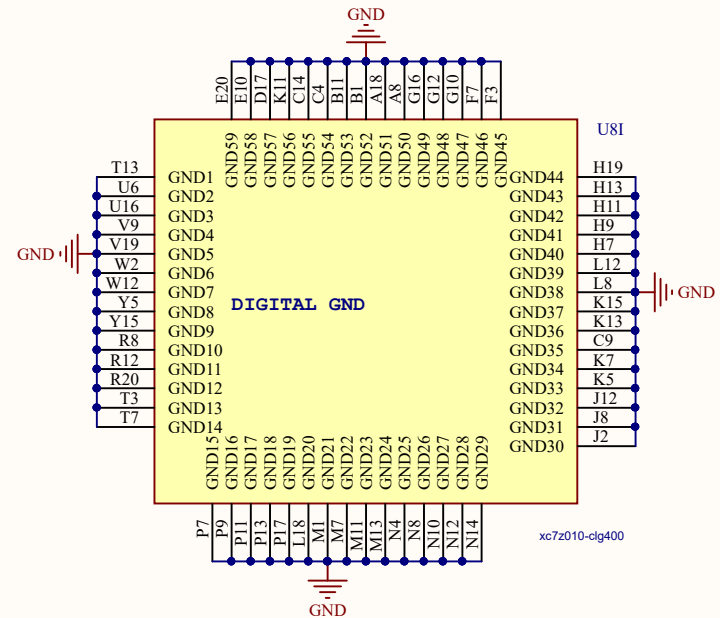
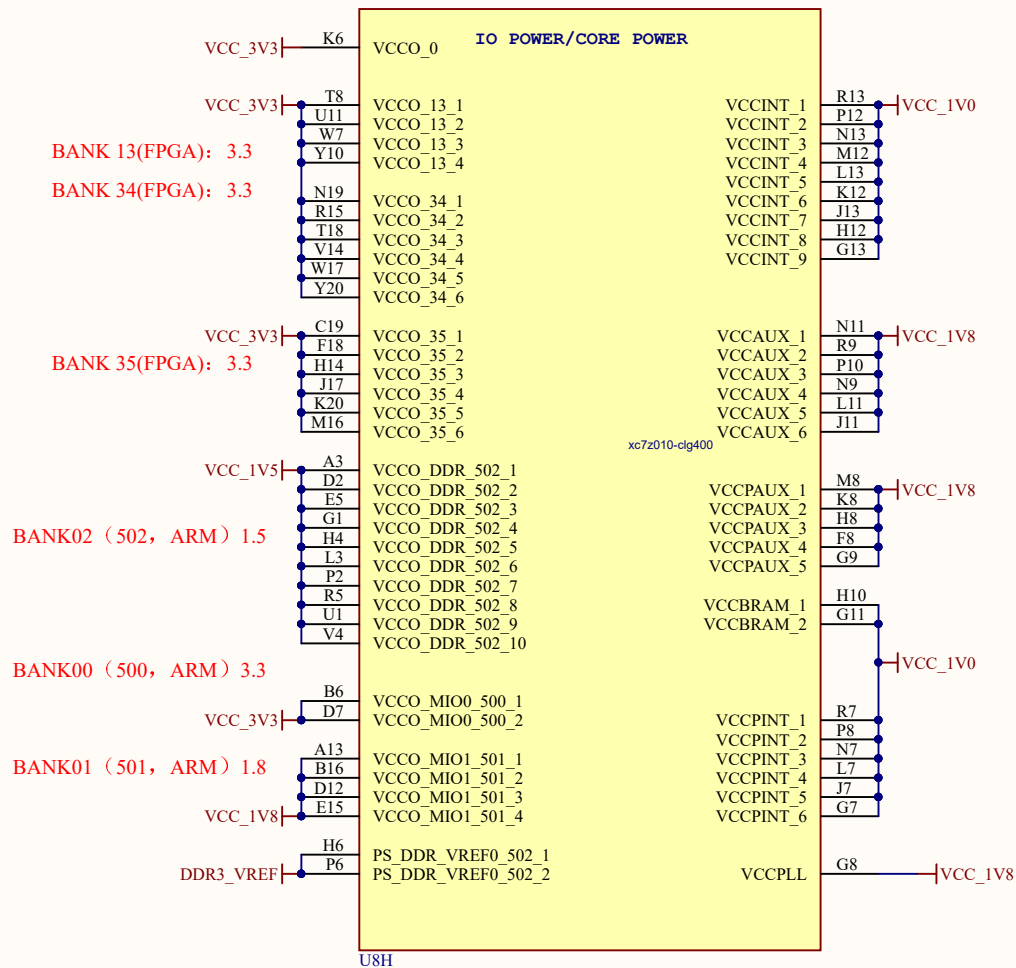


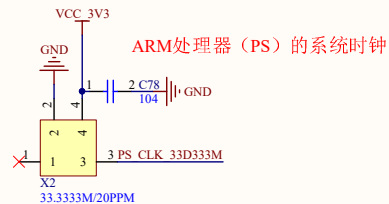
U8G



ZYNQ内核电源: 1.0V
DDR3的电源: 1.5V







ARM的bank1（501）,这个bank所有IO电平1.8V

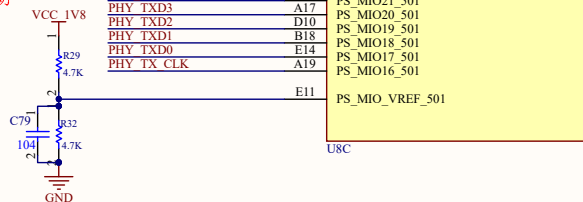
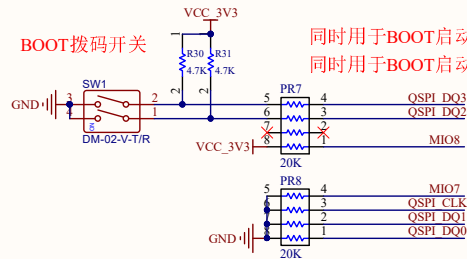
ARM的bank0（500）,这个bank所有IO电平3.3V

PS_CLK_33D333M	E7	PS_CLK_500	xc7z010-clg400
ARM_nPOR	C7	PS_POR_B_500	
SD1_D3	C8	PS_MIO15_500	
SD1_D2	C5	PS_MIO14_500	
SD1_D1	F8	PS_MIO13_500	
SD1_SCK	D9	PS_MIO12_500	
SD1_CMD	C6	PS_MIO11_500	
SD1_D0	E9	PS_MIO10_500	
MIO8	B5	PS_MIO9_500	
MIO7	D8	PS_MIO8_500	
QSPI_CLK	A5	PS_MIO7_500	BANK500
QSPI_DQ3	A6	PS_MIO6_500	
QSPI_DQ2	B7	PS_MIO5_500	
QSPI_DQ1	D6	PS_MIO4_500	
QSPI_DQ0	B8	PS_MIO3_500	
QSPI_CS	A7	PS_MIO2_500	
FPGA_PS_KEY1	E6	PS_MIO1_500	
		PS_MIO0_500	

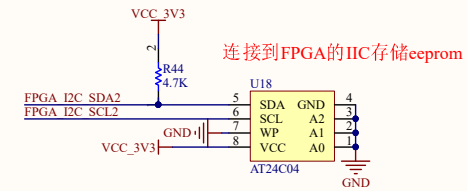
几个常用的配置MIO[5:2]:

- 1、JTAG独立配置0001，比较少用；
- 2、JTAG级联配置0000，JTAG调试常用；
- 3、FLASH启动：Quad-SPI mode，1000；
- 4、SD card：1100.

平时MIO2、3连接QSPI的存储器，状态上电默认为0
所以不用管,只管MIO4和5，两个决定是FLASH还是SD启动



VCC_1V8	1	R29	4.7K	B10	PS_SRST_B_501
PHY_MDIO	C11	PS_MIO53_501			
PHY_MDC	C10	PS_MIO52_501			
	B9	PS_MIO51_501			
	B13	PS_MIO50_501			
ZYNQ_UART1_RXD	C12	PS_MIO49_501			
ZYNQ_UART1_TXD	B12	PS_MIO48_501			
	B14	PS_MIO47_501			
USBPHY_nRSET	D16	PS_MIO46_501			
SD0_D3	B15	PS_MIO45_501			
SD0_D2	F13	PS_MIO44_501			
SD0_D1	A9	PS_MIO43_501			
SD0_D0	E12	PS_MIO42_501			
SD0_CMD	C17	PS_MIO41_501			
SD0_SCK	D14	PS_MIO40_501			
USBPHY_DATA7	C18	PS_MIO39_501			
USBPHY_DATA6	E13	PS_MIO38_501			
USBPHY_DATA5	A10	PS_MIO37_501			
USBPHY_CLKOUT	A11	PS_MIO36_501			
USBPHY_DATA3	F12	PS_MIO35_501			
USBPHY_DATA2	A12	PS_MIO34_501			
USBPHY_DATA1	D15	PS_MIO33_501			
USBPHY_DATA0	A14	PS_MIO32_501			
USBPHY_NXT	E16	PS_MIO31_501			
USBPHY_STP	C15	PS_MIO30_501			
USBPHY_DIR	C13	PS_MIO29_501			
USBPHY_DATA4	C16	PS_MIO28_501			
PHY_RXCTL	D13	PS_MIO27_501			
PHY_RXD3	A15	PS_MIO26_501			
PHY_RXD2	F15	PS_MIO25_501			
PHY_RXD1	A16	PS_MIO24_501			
PHY_RXD0	D11	PS_MIO23_501			
PHY_RX_CLK	B17	PS_MIO22_501			
PHY_TXCTL	F14	PS_MIO21_501			
PHY_TXD3	A17	PS_MIO20_501			
PHY_TXD2	D10	PS_MIO19_501			
PHY_TXD1	B18	PS_MIO18_501			
PHY_TXD0	E14	PS_MIO17_501			
PHY_TX_CLK	A19	PS_MIO16_501			
	E11	PS_MIO_VREF_501			

[illegible]

SD1

TF2

VCC_3V3

VCC_3V3

GND

R45 7k2

SD1 D2

SD1 D3

SD1 CMD

SD1 SCK

SD1 D0

SD1 D1

0

SHELD

TF_Card

Schematic diagram of the SPI interface between the ATmega328P and the W25Q256FV. The ATmega328P is shown as a yellow box with pins 1-8. Pin 1 is CS, pin 2 is DO1, pin 3 is DO2, pin 4 is GND, pin 5 is DI, pin 6 is DO3, pin 7 is CLK, and pin 8 is VCC. The W25Q256FV is shown as a blue box with pins 1-4. Pin 1 is DO3, pin 2 is CLK, pin 3 is DO0, and pin 4 is GND. A 4.7k resistor is connected between the ATmega328P pin 6 (CLK) and the W25Q256FV pin 1 (DO3). The ATmega328P pin 8 (VCC) is connected to VCC_3V3, and pin 4 (GND) is connected to GND. The W25Q256FV pin 4 (GND) is also connected to GND.

